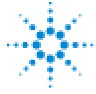

Hybrid32 Migration White Paper

REVISION HISTORY

Version 1	09/00	Original release version of the Hybrid32 Migration Whitepaper.
Version 2	11/00	Updated the “Analog Tests – Details and Debug Quick Reference” section with information on dealing with system residual capacitance. Added “Appendix D: Guidelines for using Functional Test Access Ports with the Hybrid32”.

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Introduction

The Hybrid32 Pin Card is a complementary accessory for the Agilent 3070 that offers users greater and more cost-effective digital channel testing capability. It provides twice the number of digital channels available on HybridPlus Pin Cards, helping manufacturers more economically meet the increasing test demands for large pin count **digital** devices while protecting their existing investments in test programs, fixtures, and training.

This document is provided to help users of HybridPlus Pin Cards more easily incorporate the Hybrid32 technology into their existing systems and to continue to provide and support the high level of test transportability provided by the 3070. It describes similarities and differences between the Hybrid32 Pin Card and previous Pin Cards, and provides tips and recommendations on migrating to the Hybrid32 Pin Card.

Adding Hybrid32 Pin Card technology is a relatively straightforward process, if appropriate steps are taken during migration. Some initial effort is needed to review and debug test programs. You are encouraged to use the streamlined Board Grader procedure provided (Appendix C) to expedite identification of marginal analog tests.

The following naming conventions are used when referring to Pin Cards:

Hybrid Single Density: Single density Pin Card with 8 channels.

E400xA: First generation of 16 channel double density (easily identifiable in the DGN screen as one of the following: "H_StdDD", "H_AdvDD", "H_HA_DD", "H_PpuDD").

E400xB: Second generation of 16 channel double density (easily identifiable in the DGN screen as one of the following: "HStdDD2", "HAdvDD2", "HHA_DD2", "HPpuDD2").

HybridPlus Pin Cards: E400xA and E400xB double density Pin Cards with 16 channels.

Hybrid32: New 32 channel Pin Card with 32 channels (easily identifiable in the DGN screen as one of the following: "HStd_32", "HAdv_32", "H_HA_32", "HPpu_32").

Note: DGN card abbreviations represent functional speeds as follows:
"Std" = 6MHz, "Adv" = 12MHz, "HA" = 20MHz, "Ppu" = Pay Per Use

Hybrid32 Overview

- The new "Hybrid32" Pin Card has two distinct operating modes – 16 Channel Mode operation and 32 Channel Mode operation. The 16 Channel Mode operation preserves your investment in existing test programs and fixtures. The 32 Channel Mode operation allows you to take advantage of additional **digital** channels in future test program development. A combination of both Hybrid32 and HybridPlus can be mixed in an appropriately configured 3070 system (see System Requirements below).

System Requirements

Hybrid32 requires systems that:

- Run software revision B.03.80 or greater.
- Contain only ControlXT cards.
- Have Series II original fans or Series 3 blowers (no original Series 3 or Series 2 upgraded fans).
- Do not currently contain Serial Test Cards (STC or STC+).
- Run on the UNIX platform.

16 Channel Mode Operation

- The Hybrid32 is used in the system in place of existing E400xA/B HybridPlus Double Density Pin Cards or Single Density Pin Cards.
- When running in 16 channel mode, the Hybrid32 maintains a very high-degree of backward compatibility for existing customer test programs developed for the HybridPlus Double Density or Single Density Pin Cards.
- The Hybrid32 performed very well in beta site testing where existing customer test programs were migrated to Hybrid32 Pin Cards. At three customer sites, the migration process achieved a passing test rate of **99.6%** for analog tests and **99.1%** for digital tests.
- However, you should expect migration efforts to be typically 2-5 hours on most of their test programs, depending on the robustness of their tests and the experience level of their test engineers.
- At customer beta sites, 17 of 20 testplans required some debug, typically failing 2-4 analog tests and 2-5 digital tests per testplan.
- The Board Grader "Lite" procedure described in Appendix C is an effective tool for evaluating and improving the performance of analog tests.
- Agilent 3070 Users can expect 100% existing **physical fixture** migration to the Hybrid32 Pin Card for fixtures designed for the existing E400xA/B HybridPlus Double Density Pin Cards or Single Density Pin Cards. As noted previously, test program migration is likely to require some debug effort as described in this document.
- Hybrid32 cards can be used in the same module as ChannelPlus cards, but a Hybrid32 card **is not a replacement for a ChannelPlus Pin Card with existing fixtures**. (Further details are provided in the next section.)
- Testhead configurations containing the combination of Hybrid32 and Serial Test Card (STC or STC+) are not currently supported.

32 Channel Mode Operation

- Digital channel count doubles when using the Hybrid32 in the 32 channel mode. The extra digital channels provided by the Hybrid32 add value for manufacturers who need more digital resources (drivers and receivers for digital tests).
- Hybrid32 ***does not*** add extra node count or capacity for analog capabilities beyond those supplied by HybridPlus Pin Cards because the number of fixture-to-tester interface pins and analog buses remains the same.
- Hybrid32 Pin Card provides twice the number of **digital** channels with full functionality of overdrive and programmable drive and receive levels. This makes the Hybrid32 an improved and more viable **high channel count** solution than the previous ChannelPlus card. However, 3070 Users must understand that because the Hybrid32 card cannot emulate the multiplexing scheme (i.e., no pin-to-pin relationship) of a ChannelPlus Pin Card, the Hybrid32 Pin Card cannot directly replace existing ChannelPlus Pin Cards.

Similarities between Hybrid32 and HybridPlus Pin Cards

- Hybrid32 will support all the existing features currently supported for the E400xA/B HybridPlus Double Density Pin Cards.
- The number of MINT pins (fixture to tester interface pins) remains the same – two rows of 78.
- The use model for development software and debug software is the same as for the existing Pin Cards. The customer preserves the value of their previous training and knowledge, which can now be utilized with the Hybrid32.
- The customer can re-use existing test programs developed for previous HybridPlus Double Density and Single Density Pin Cards with limited debug (typically 2-5 hours) (see Appendix C for Board Grader "Lite" procedure).
- Test Specifications as described in the Agilent 3070 Users' Manual, Board Test Fundamentals, Chapter 6 Test Specification are not changed by the addition of the Hybrid32 Card.
- Testplan throughput speed is maintained. The testplan execution time on the Hybrid32 Pin Cards running in 16 channel mode is as fast as that of the existing Pin Cards.
- Relay Diagnostics is supported for the Hybrid32 card as it is for the HybridPlus Pin Cards. Agilent CEs and Co-operative Support Customers will be able to continue using Relay Diagnostics to repair cards in the field when possible.
- Service documentation is available on line with your Agilent 3070 system software.
- Power consumption is the same as HybridPlus Double Density cards.

Differences between Hybrid32 and HybridPlus Double Density Pin Cards

- Digital channel count doubles to 32 from 16 when using the Hybrid32 card in 32 Channel Mode.
- New DGN tests have been added to test the Hybrid32 card's additional functionality (13xxx range).
- DGN and autoadjust execution time on Hybrid32 is approximately twice as long as DGN and autoadjust execution time on E400xA/B HybridPlus Double Density because of the extra channels tested.
- Hybrid32 card requires a Control XT control card.
- Hybrid32 card currently is not supported in systems with serial cards (STC or STC+).
- Software required is B.03.80 or greater.
- Cooling configuration required is blowers or original Series II fans (no original Series 3 or Series 2 upgraded fans).

Migrating Between Hybrid32 in 16 channel mode and HybridPlus Double Density Pin Cards

Running existing Testplans on Hybrid32 Pin Cards

- For the smoothest migration effort, proactively review your test programs for robustness using the Board Grader "Lite" procedure in Appendix C.
- Before using the Hybrid32, customers should meet the system requirements as defined above. Hybrid32 card installation can be performed by Agilent CEs or trained Co-operative support customers.
- The existing board directory and test objects will not need to be modified or recompiled except for the limited number of test objects associated with test sources that may need to be debugged.
- No change is needed for the board config file. Do not modify the ***board config*** file with its existing HybridPlus syntax. This syntax will put the Hybrid32 card into 16 channel mode when the ***'load board'*** command is executed. Run the testplan.
- Users do not need to change the control card type in the ***board config*** file when using existing testplans with Hybrid32 in the 16 channel mode.
- Users upgrading existing testplans to ControlXT cards to take advantage of the added functionality and speed should refer to the Incremental Training Guide for B.03.00 in the on-line Users' Manuals for ControlXT card upgrade information.
- Most test programs may require some limited amount of debugging depending upon the robustness of the tests. This could involve 2-5 hours of effort for an estimated 2 – 4 analog tests and 2 – 5 digital tests per test program. (See Appendix C)

Focusing and Minimizing Hybrid32 Migration Effort

- Beta Site results indicate that more than 99% of existing analog and digital tests will migrate smoothly to the Hybrid32 Pin Cards.
- However, most existing test programs debugged or currently running on the existing HybridPlus cards will require some debugging to migrate to Hybrid32 cards.
- This will typically take an estimated 2-5 hours per failing test program.
- At customer beta sites, 17 of 20 testplans required some debug, typically failing 2-4 analog tests and 2-5 digital tests per testplan
- See Appendix C for migration minimization tool Board Grader "Lite ".
- Users who have effectively used Board Grader or their own custom test program qualifier to identify and fix marginal tests before they appear during production will have a higher level of robustness in their current programs.
- Board Grader identifies those tests that are close to failing because of uncentered means, low reproducibility, and marginal dependence on drive/receive levels.
- Appendix C contains a simplified procedure for using Board Grader to readily identify analog tests that are not robust.
- Test trends – tests most likely to need debug effort:
  - Analog tests that have poorly centered means and low coefficients of reproducibility.
  - Tests that are unstable in existing testplans are likely to be unstable on systems with Hybrid32.
  - Digital tests that rely on unspecified Pin Card parasitics/parametrics to float digital outputs or inputs to a certain state rather than explicitly defining the desired states.

Analog Tests – Details and Debug Quick Reference

The following suggestions are provided as a general basis for adjusting existing analog tests that may fail when migrating to the Hybrid32 Pin Card. The exact remedy for a specific failing component will depend on the actual circuit topology. Tests with well-centered means and good reproducibility generally will not require any debug. Users can use the Board Grader "Lite" procedure included in Appendix C as a preventive measure to avoid analog test failures. Refer to the onboard Agilent 3070 User's Manual, Test Methods: Analog, Chapter 5 Debugging Analog Tests for more information and details on debugging analog tests.

- Use capacitor compensation for small value capacitor measurements to take out system variability due to residual analog bus capacitance. The analog bus capacitance is specified to be 0 to 40pF (typical) for a fully loaded module of pincards (any combination of Hybrid32 or HybridPlus pincards). Capacitor compensation can be used to account for shifts in residual bus capacitance between pincards. The Board Grader "Lite" procedure included in Appendix C can help identify marginally passing tests that could be affected by system residuals.

- Change feedback on the MOA to reflect circuit topology. This is ideally as close as possible to the value of the impedance being tested. Valid feedback options are re1...re6. For tests with high guard ratios, smaller feedback resistors may be used to reduce the guard gain error.
  - When debugging resister tests choose the "re" option and the "am" option to maintain an MOA gain of 1 to 10 and an MOA output of .1 to 1 volt. Use "Display MOA" in the Analog Debug Menu to look at the MOA output and source loading. See the Agilent 3070 Users' Manual, Test Methods: Shorts and Analog, Chapters 3 and 5 for further details

- For capacitors reading a lower value than expected, increase the source amplitude to 0.2v. Ensure that semiconductor junctions of common devices on the source node will not turn on using 0.2v.
- Use "ed" for line noise rejection if the suspected cause of measurement instability is line noise.
- Add guarding and enhancement for low impedance component tests. Beware that an increase in measurement accuracy with the "en" or "ed" options will result in increased test times.
- Change frequency of the test ("fr" option) for reactive components so that the DUT is the dominant impedance being tested. Valid frequency options are fr128, fr1024, and fr8192. Note that fr128 requires use of "ed" option.
- Use IPG to regenerate the test if you suspect that the test has been modified in error. Individual tests can be regenerated using the "ipg on" statement described in the Agilent 3070 Users' Manual, Syntax Reference.
- Run Pushbutton Debug "display histograms" and "display measurement" to visually inspect how well the test is centered within the limits and the corresponding coefficient of reproducibility. It may be necessary to adjust the test limits for the given circuit topology. Watch for receivers connected to non-digital pins of a device in such a way that the device functionality could be affected. An example of this would be a pull-up on a voltage reference monitoring pin.
- Swap S & I buses. Also, inspect that the S or I bus nodes are not guarded with the G bus.
- Guard as close as possible to the DUT. Changes in this area could require fixture changes.

Digital Tests – Details and Debug Quick Reference

The following information is provided as a general starting point for troubleshooting digital tests, especially those that exhibit intermittent behavior.
Beta sites and past customer data have shown that digital migration failures are primarily to the result of a few causes. The "Diagnose Faults" debug option is an excellent tool to use as a starting point for digital failures, because it will automatically vary signal levels and timing. Also, consult the Agilent 3070 User's Manual, Test Development Tools, Chapter 4 Agilent Pushbutton Debug and Test Methods: Digital, Chapter 6 Debugging Digital Tests for more debug information and details.

Floating pins

A digital test may be relying on pull-ups/pull-downs on the Pin Card to float digital outputs/inputs within a specified time. The exact time will vary with changes in customer board or 3070 Pin Card parasitics. This can cause digital tests to exhibit intermittence from one board to another or during Hybrid32 migration
Potential remedies:

- Make the vector cycle/receive delay time longer.
- Add a "keep" vector before receiving.
- Explicitly control pins using the Unit Disabling Technique described in the Agilent 3070 User's Manual, Test Methods: Digital and Syntax for conditioning.
- Add default settings on inputs to the device being tested, especially when the inputs are coming from outputs of disabled devices upstream of the tested device. See the "assign to" statement and the "default" option for this statement in the Agilent 3070 Users' Manual, Syntax Reference for details.

Receiver ringing

Slight changes in Pin Card parasitics may exacerbate a ringing problem when the digital test does not have enough margin in receiver threshold levels, receive delays, or vector cycle times. Extra ringing can cause longer settling times or unexpected clocks when ringing levels approach device thresholds.
Potential remedies:

- Adjust receive threshold levels or receive delays/vector cycle time.
- Turn receiver terminators on.

Ground Bounce

Slight changes in Pin Card parasitics may exacerbate a ground bounce problem in a large, marginally passing digital test.
Potential remedy:

- See Appendix B for tips on identifying and mitigating ground bounce problems.

Misidentified component family

The digital test has incorrectly identified the logic family (TTL, CMOS, etc) for a device, potentially changing the expected drive/receive levels.

Potential remedy:

- Correctly identify the logic family and adjust drive/receive levels as necessary.

Marginal timing

When the timing for the digital test is passing marginally, slight changes in components on customer boards or Pin Card parasitics might cause the test to behave intermittently.
Potential remedies:

- Adjust slew rate for drive signals where transition speed or transmission line characteristics are critical.
- Use receiver terminators where applicable. However, keep in mind that use of receiver termination can add some extra capacitance to the test.
- Adjust vector cycle time and receive delays.

Considerations for New Development

Specifically Targeting the Hybrid32

- Users who need more digital testing resources will benefit from the additional 16 digital channels available on the Hybrid32 for testing.
- Test programs can target systems that contain a mixture of Hybrid32 and any other Pin Card except STC and STC+ which are currently not supported with the Hybrid32.
- Test programs can target systems that are exclusively configured with Hybrid32 Pin Cards.
- As always, you must consider all systems that the test program will be expected to run on when developing test programs.
    - The board **config** file must target a system that is either equal to or a subset of each of the systems that the program will eventually be executed on. This is critical to ensure that IPG will correctly assign only resources available on the targeted machine.
    - The Hybrid32 Pin Card, in 32 channel mode, is not a subset of any other existing card. Once a test program and fixture are developed to run a Hybrid32 in 32 channel mode in specific card slots then that fixture and test program must always have a Hybrid32 available in those specific spots. See the Agilent 3070 Users' Manual, Cards in the Testhead, Chapter 3 System Configuration for more details on system subsets.
- New testplans that specifically target the Hybrid32 may result in fewer Hybrid32 Pin Cards in the testhead compared to the same development that targets the HybridPlus Pin Cards.
- The higher digital resource to ground ratio on the Hybrid32 cards may increase ground bounce sensitivity.
    - When more test resources are concentrated on fewer Pin Cards, the testplan and fixture development should be proactive to avoid ground bounce and fixture problems. See Appendix B for tips on preventing ground bounce.
    - The general best practices for fixture design and program development discussed in Appendix B should always be followed to minimize ground bounce sensitivity.

Targeting HybridPlus Double Density Systems in Test Program Development

- Consistent with the current development use model, systems containing Hybrid32 cards provide the flexibility to develop test programs targeting systems whose functionality is a subset of the Hybrid32.
    - The board **config** file must target the system that the program will eventually be executed on. This is critical to ensure that IPG will correctly assign only resources available on the targeted machine.

    - The board **config** file must be equal to or a subset of the testhead **config** file of the machine that you are developing on to allow for debugging.
- For best migration to the targeted machine, use test qualifying tools such as Board Grader or Qstats to qualify test robustness.

Sharing Test Programs between Hybrid32 Systems and HybridPlus Double Density Systems

The strong test transportability provided by 3070 systems is a key to success in an environment where programs and fixtures are moved among testheads frequently.

- Test robustness is especially valuable for test programs that will run on machines with different but functionally equivalent configurations.
- For best migration and ease of maintenance, test programs running in this type of environment should be qualified for test robustness using tools such as Board Grader, Qstats, or custom qualification programs.
- Beta site studies indicated that test programs that have not been thoroughly qualified for robustness may have a limited number of tests that will need to be debugged on both systems to ensure that test option adjustments (i.e., “en”, “re4”, limit shifts, etc.) will run on both systems.

Appendix A: Hybrid32 Beta Site Summary Results

Beta Site #1 (3 testplans, 1 required debug)

analog failures = 1/4558 = 0.022%
digital failures = 1/1322 = 0.076%
Beta Site #2 (10 testplans, 9 required debug)
analog failures = 12/5432 = 0.22%
digital failures = 20/1498 = 1.34%
Beta Site #3 (7 testplans, 7 required debug)
analog failures = 49/6300 = 0.78%
digital failures = 7/301 = 2.3%

Totals (20 testplans, 17 required debug)
analog failures = 62/16290 = 0.38%
digital failures = 28/3121 = 0.9%

Appendix B: Ground Bounce Background and Guidelines

What is it?
Ground Bounce Definition: A transient voltage differential between the test system ground and the DUT ground. Signal lines from the tester to the DUT are referenced to the 3070 ground. When ground bounce happens, it appears as if a similar, but inverted transient pulse appears on signal lines at the DUT as referenced to DUT ground. Signal lines such as clock inputs and asynchronous reset lines are particularly vulnerable to such transients.

How do you identify it?

- Use a high-speed digital storage scope to compare actual and expected DUT outputs and look on sequential circuits for glitches on DUT clock and reset inputs.

  - Ground bounce scope tips - It's very important to use good measurement methods, including a high performance scope and good scope probing techniques.

    - Measure the symptoms of ground bounce by "scoping" transient-sensitive DUT inputs with respect to DUT ground.

    - Use a VERY short scope probe ground connected directly to a DUT ground point VERY close to the DUT input. Ground bounce will usually be coincident with a test event in which many signal lines change state, especially lines with high current (e.g. backdriven lines) and/or high slew rates.

  - Ground bounce will exhibit a "bouncing" effect for the signal at the DUT resulting in a hard or intermittent test failure.

    - Ground bounce should not be confused with receiver ringing problems where an "ringing" effect is seen at the input to the pincard receiver. The ringing will eventually settle to the correct state if a wait period is added to the test. Ground bounce problems are different in that they are not simply solved by waiting for signals to settle. Receiver ringing problems can be handled with the methods suggested in the Digital Tests – Details and Debug Quick Reference portion of this paper.

    - Problems occurring due to ground bounce typically appear on transient sensitive inputs before the actual failure either within the failing vector or at some point previous to the failing vector. Scope analysis should be focused on suspected transient sensitive inputs previous to the failure. Read on for suggestions on addressing ground bounce.

Typical potential ground bounce situations:
Ground bounce can be the result of various interactions between the tester and the board under test.

- Simultaneously switching states on large numbers of DUT outputs with 3070 receivers connected or even without receivers connected but with large numbers of nails (probes not used in that test) connected in a single test. There is some loading associated with connecting a receiver. There is still some loading associated with probes connected to nodes even when no driver or receiver resource is connected for that test. When outputs to a large

number of receivers or probed nodes are switched from one level to another simultaneously, the result may be signal glitches at the DUT's input signals due to the board ground and tester ground relationship being momentarily impacted.
- Large number of drivers that are back driving being tri-stated simultaneously.
- Both of the above are made worse by faster chips, higher currents, all 1 to 0 or 0 to 1 transitions

Ways to address ground bounce:

Typical methods of addressing ground bounce issues:

- Add a ferrite bead to reduce the loading (raise the inductance) of receiver wires or wires attached to probed nodes connected to the DUT outputs. This will reduce the ground bounce transients. However, this will slow the slew rate of signals to these nodes and make it difficult to backdrive on this node.
- Reduce unnecessary loading by removing probes or using dual stage probes on DUT outputs that are not used in the test.
- Reduce total number of pins transitioning at one time by segmenting large tests into smaller tests.
  - Manually examine the DUT specifications and VCL code to determine which outputs can be operated independently. Strategically group the outputs that must act together into several smaller tests.
  - Segment Connect Tests using Max Connect auto breakup feature. See the Agilent 3070 User's Manual for details on this feature.
- Reduce the potential for transients by balancing the states of the transitioning pins. Edit the test to try to equalize the number of pins transitioning high at a specific time with the number of pins transitioning low at that time.
- Reduce the potential for transients by staggering the tri-stating of large numbers of pins.
- Reduce the amount of current at a given time by utilizing upstream disabling.
- Reduce 3070 driver slew rates. Driver slew rates do not cause ground bounce problems, but slowing the slew rate for a test may reduce the sensitivity of the test to ground bounce. Note that slew rates should only be slowed if the component under test allows.

Preventing ground bounce for new fixtures:

- Declare nodes that are expected to be sensitive to ground bounce (clocks, resets, etc) as critical nodes so the fixture development software will assign shorter wires between Pin Cards and the fixture for those signals. Be especially conscious of wire lengths and board placement when using Shared Wire fixtures and topside probing, as it may be necessary to relocate critical resources.
- During the board design phase, make sure that ground connections on the DUT are freely available for access by the fixture. Good ground integrity (low impedance) between the fixture and the DUT is as important as the ground integrity between test system Pin Card resources and the fixture.
- Use twisted pair wire for the critical signals.
- Set the Ground Bounce Suppression option to "ON" in the IPG Global Options form in the test development software when developing Boundary Scan tests. This option will add some additional test vectors in order to steer the chain through a state path that increases test immunity to spurious clocks.

- Try to make sure that critical signals (such as TCK and TRST and possibly TMS for Boundary Scan) use resources on Pin Cards that have an ample number of grounds. If possible, assign critical signals to less utilized Pin Cards.
- Make sure that grounds aren't blocked, especially on Pin Cards that provide resources for critical signals. The your_board_directory/fixture/details file will provide information on scarce resources.
- Reduce the inductance of the ground return path with a ground plane.

Appendix C: Agilent 3070 Board Grader "Lite" Procedure

Purpose

This procedure describes how to use the 3070 Board Grader software in a way that it only looks at shorts, pins, and analog tests. This method of applying Board Grader in a time saving, analog focused manner is useful for circumstances where test program robustness is desired but time investment must be minimized. It is also useful when most of the needed improvements are expected to be in the analog section. However, for circumstances requiring test program robustness to be thoroughly maximized across all tests, Board Grader should be used in its entirety.
Normally, Board Grader will look at all tests in the testplan. However, digital and mixed tests will be recompiled with the "debug" option so that sensitivity to drive/receive levels and vector cycle/receive delay times can be tested. This recompile step can take a significant amount of time. When examining test programs for robustness with respect to transportability, we may only want to know about the analog incircuit portion of the testplan. In general, most transportability issues arise around analog tests.

Prerequisites

Before starting this procedure, you should have a good understanding of the purpose and procedures for running the 3070 Board Grader software. This can be found in the 3070 manuals under "Test Development Tools" and specifically chapter 9 titled "Board Test Grader & Test Coverage." Additional information can be found in the "Previous Incremental Training Guides" section of the on-line manuals under "Revision E (B.02.75)". There is important information related to running the Board Grader software on a panelized board in the incremental training guide not found in the "Test Development Tools" manual.

Detailed Procedure

The following is the detailed procedure for doing an 'analog-only' Board Grader test. Most of this is from the manuals.

1. Using "**vi**" or the BT-Basic editor, create a file named "**comment_digital**" with the following code in it. This is a "Perl" script that will modify your testplan to comment out any uncommented lines with '**test "digital/'** or '**test "mixed/'** in them. This file will be used for every board you want to run the Board Grader "Lite" procedure on.
   You will want to save it in a directory that everyone will be able to find it. The directory **/usr/local/bin** has read-write access for everyone and is in the search path for all users, so place the "**comment_digital**" file in that directory.

```
#!/bin/perl
#
# script to comment all the lines that start with:
#
#     test "digital/"   and
#     test "mixed/"
sub print_usage {
   print "USAGE: comment_dig -i <inputfile>\n\n";
   print "where  -i  specifies an input file name.\n";
   exit ;
}
while ($_ = $ARGV[0], /^-/) {
   shift;
   if (/^-i/) {
      if ( $#ARGV < 0 ) {
         print "ERROR: No input file name specified.\n\n";
         print_usage ();
      }
      if ( not -e $ARGV[0] ) {     # Check to see that the file exists.
         print "ERROR: The input file $ARGV[0] does not exist.\n\n";
         print_usage ();
      } else {
         $infile = $ARGV[0];
      }
      shift;
      next;
   }
   print "ERROR: Invalid option specified: $_ .\n\n";
   print_usage ();
}
# Main program starts here.
open (TP, $infile) or die qq(ERROR: Cannot open "$infile" for reading.\n) ;
while ($line = <TP>) {
# Search for lines that start with 0 or more white space characters followed
# by the word 'test' followed by 1 or more whitespace characters followed by
# either '"digital/' or '"mixed/' and print that line preceded by "!BDG_LITE".
   if ( $line  =~  /^\s*test\s+"digital\// or $line  =~  /^\s*test\s+"mixed\// )
{
         print "!BDG_LITE $line";
   } else {
         print "$line";       # Otherwise, just print the line as it is.
   }
}
```

2. Save this file and, from a shell prompt, do a **chmod 755 /usr/local/bin/comment_digital**. This sets the permissions on the file such that you can execute it.
3. Get your testplan to the point that it will pass boards prior to running the Board Grader process on it. In particular, find a board that passes all the time. Board Grader statistics measure the test robustness on a single board to eliminate the variables introduced board to board and focus on the individual test strength. If you cannot find one that passes, find a board that passes most of the time. Board Grader analysis will "flag" failing tests in its reports and you can look at the flagged tests to see if they correspond to known failing tests.
4. From the BT-Basic command line, run **grade tests; configuration**. This creates the Board Grader configuration file (**config.bdg**).
5. Load the Board Grader configuration file into the Basic workspace (**load "config.bdg"**).
6. Search for the section labeled "**# Digital Incircuit Test Options**". Modify this section of the file to turn off all the tests done in that section. To do this, each variable that ends in "**_Test**" should be set to "**False**". An example is shown below:
   Digital_Incircuit_Vacuum_Off_Test = False
7. Repeat step 4 for the sections labeled "**# Digital Functional Test Options**" and **"# Analog Functional Test Options**". Re-save the "**config.bdg**" file.
8. **Important!** Make a copy of your original testplan. Please always back up your working copy of any file or directory before experimenting. From the BT-Basic command line:
   copy "testplan" to "testplan.pre_bdg"
   Or, from a Unix shell prompt:
   cp testplan testplan.pre_bdg
9. From a shell prompt, run the following command:
   comment_digital -i testplan.pre_bdg > testplan
   This will create a file named "**testplan**" (or overwrite the existing testplan file) with the digital and mixed lines commented out from the input file named "**testplan.pre_bdg**" (created in step 8 above).
10. You can now run the command **grade tests; testplan** from the BT-Basic window. This will create the shorts tests with different thresholds and settling delays and compile them. In addition, a board grader testplan is created (**testplan.bdg**). This is what you will run to actually do the board grader testing on the analog components. Because we ran the **comment_digital** script, no digital or mixed compiles should occur. If they do, check the **testplan** file to make sure that all '**test "digital**' or '**test "mixed**' lines are commented out. The script will comment the line with a "**!BDG_LITE**" comment.
11. You can now load and run the board grader testplan (From the BT-Basic prompt, do **load "testplan.bdg" | run**). Be aware that vacuum will be removed and applied throughout the testplan execution. You need to make sure the board is seated on the fixture properly. If you have errors running the testplan, check the troubleshooting section of the Board Grader manual in the on-line 3070 User's Manuals.
12. Once the testplan has finished running, generate the board grader reports by running the command **grade tests; report** from the BT-Basic command line. The report files (by default) will be created in the **bdg_data** directory. Now you have the data that will assist you in identifying potential migration issues and focusing your debug efforts with the most effect. See the "**Analysis of Board Grader Data**" section for the discussion of what to look for in this data.

Important Notes

Below are some specific things to watch for when trying to execute this procedure. These include issues for versioned boards as well as panelized or dual-well shared-wire fixtures.

Versioned board

- Do a '**load board**' followed by a "**board version is ***" or "**board version is <version>**" prior to doing a "**grade tests; testplan**". This sets the board version so that the compiles run without errors.

Panelized or Dual-well shared-wire board:

- In the "**config.bdg**" file, edit the following:

  Boards_on_Panel = <= Enter the number of boards on the panel.

  Test_Board_Number = <= Enter the board number in the panel to test.

- If a Dual-well fixture (operating from separate vacuum sources), modify the "**Dual_Well_Enable(N)**" variables accordingly (for example, 2 wells would have "**Dual_Well_Enable(1)**" and "**Dual_Well_Enable(2)**" both set to "**True**").

Analysis of Board Grader Data

After executing the board grader testplan and creating the report files, look at the results. Start with the **summary.rpt** file first. Look for tests that are "Flagged" and those that are listed as "Unsuccessful". A "Flagged" test is one that may not be centered between the limits or the Cpk is below a specified threshold. An "Unsuccessful" test is one that failed when it should have passed or one that passed when it should have failed. For example, all tests in the Analog Incircuit Quality section should pass. Likewise, all tests in the Analog Incircuit Vacuum Off section should fail. "Unsuccessful" tests should always be debugged. "Flagged" tests are those that might not migrate well and should be debugged

Details of what specific test failed are shown in the individual reports for the test section. For example, the report for the Analog Incircuit Quality section of Board Grader is located in the **ana_inc_qua.rpt** file located in the **bdg_data** directory.

An example of the summary report (**summary.rpt**) is shown in Figure 1. Note that this summary report was for a full run of the Board Grader software (digital and mixed tests are included).

```
----------------------------------------------------------------------------------
HP3070 BOARD TEST GRADER                      Fri Apr 14 10:27:50 2000  page 1
SUMMARY REPORT
----------------------------------------------------------------------------------

Board Path:               ./
Board Serial #:           Board1

Test                                          Number Number  Number    Number
                                              Total  Success Unsuccess Flagged
Pins                                              10      10         0
Pre-Shorts                                       450     450         0         1
Shorts                                            50      50         0
Analog Incircuit Vacuum Off                      293     293         0
Digital Incircuit Vacuum Off                       8       8         0
Analog Functional Vacuum Off                      29       8        21
Analog Incircuit Quality                        2930    2919        11        57
Digital Incircuit Quality                         90      90         0         0
Analog Functional Quality                        300     300         0         3
Digital Incircuit Power Supply Sensitivity        16      16         0
Analog Functional Power Supply Sensitivity         8       8         0
Digital Incircuit Speed Sensitivity               16      16         0
Analog Functional Speed Sensitivity                2       2         0
Digital Incircuit Logic Level Sensitivity        364     364         0
Analog Functional Logic Level Sensitivity          0       0         0
Digital Incircuit Fault Coverage                 546     495        51
Analog Functional Fault Coverage                   0       0         0
```

Figure 1. Example of the Summary report (**summary.rpt**).

Of particular interest for the Board Grader "Lite" procedure is the Analog In-Circuit Quality report (**ana_inc_qua.rpt**) because digital and mixed tests are ignored for this procedure. Figure 2 shows the Analog In-Circuit Quality report. Some things to note on the report:

- Note that there is a good explanation of the column headings at the end of this file. Make sure you understand what each of the columns is for. Also, the "Flagged" column (labeled "**# Flg**") will be described at the top of the section. Look for the line starting with "**Report Flags:**".
- The first section will be for jumper tests. The jumper test is looking for the resistance measurement to be above or below a specified threshold. Because no limits are part of the test, it cannot be treated like a resistor as far as a Cpk value is concerned. Simply look at the "Flagged" column for tests to check further. Again, "Flagged" tests indicate tests that will potentially not migrate well. These tests should be debugged.
- Watch for devices that have a "F" next to them. These tests failed during the run of the testplan. These devices probably are intermittent failures on the board.
- Also, watch for devices that have a small value, but have very large limits. Make sure the test is valid. An example would be a capacitor that has a nominal value of 5pF, but has low limit of –2000pF and a high limit of 19pF. This should not be tested, as the 3070 would not be able to detect whether the capacitor is installed. Use the "**pc**" option for small value capacitors in debug to see if the reading is valid.

Analog Incircuit Quality REPORT

Board Path: ./
Board Serial #: Board1
Date of Data generation: Wed Dec 31 16:59:59 1969
Number of test runs (in config.bdg): 10
Number of tests: 390
Report Flags:

F = Test failed
N = Margin too small 2.00 , 100.00

Designator	Programmed Thr.	OC	Computed Mean	Computed StdDev	Computed Margin	# Pass	# Fail	Flg	Com Ref
r39	100k	O	42.3M	31.5M	-40.2M	10	0	N	...
r93	100k	O	-40.1M	0	-40.2M	10	0	N	...
r362	10.0k	O	1.58M	90.6k	1.49M	10	0		...
r502	1.00k	O	-34.4M	17.9M	-40.1M	10	0	N	...
r500_op	1.00k	O	27.6M	15.7M	15.4M	10	0		...
r501	1.00k	O	39.7M	12.8M	15.4M	10	0		...
r372	1.00k	O	-40.1M	0	-40.1M	10	0	N	...

Report Flags:
F = Test failed
M = Mean not centered 66.67%
C = Coefficient of producibility too small 10.00

Designator	Programmed Nom	Programmed Low	Programmed High	Computed Mean	Computed StdDev	Computed CPK	Computed CP	# Bad	Flg	Com Ref
c11	33.0p	16.5p	116p	33.1p	20.0p	277m	827m	1	CF	...
c228	33.0p	26.7p	60.5p	53.1p	4e-14	60.8	138	0		...
c237	20.0p	16.2p	56.7p	42.7p	3.30p	1.40	2.04	0	C	...
c245	390n	310n	470n	375n	29.5p	731	902	0		...
cr1:cr1_2	N/A	225m	856m	757m	156u	212	676	0	M	...
cr2:cr1_2	N/A	225m	856m	758m	107u	303	980	0	M	...
r319	1.00	-366m	2.27	52.0m	609u	229	722	0	M	...

The columns have the following meaning:

- Designator: This is the main device designator. If a device test has several test statements (e.g. diode tests on the emitter-base and base-collector junctions of a transistor) a sub-designator is added
- Thr: The threshold for determining an open or closed result.
- O/C: Open or closed, depending on the test.
- Nom: The nominal value in the test statement.
- Low: The lower limit in the test statement.
- High: The upper limit in the test statement.
- Mean: The mean of the values obtained by repeating the test.
- StdDev: The standard deviation of the obtained by repeating the test.
- Margin: The difference between the threshold and the closed measurements.
- CPK: The coefficient of producibility. CPK greater than 10 provides confidence in the producibility and stability of the test.

CP: The minimum value where the CPK is determined by the limit closest to the mean. CP is equal to CPK where the mean is centered.
 # Bad: The number of times the test failed.
Flg: These columns will have a warning flag character in the corresponding column (e.g. M if the mean is not centered in the limits band).
Com Ref: This will allow the user to enter the comment number specified in the comment files.

Figure 2. Example of the Analog Incircuit Quality report (`ana_inc_qua.rpt`).

Conclusion

While the Board Grader software may seem somewhat complicated to use, it provides very useful information to the programmer. This information is used to create a robust and transportable program and fixture. In addition to transporting well, robust programs can also minimize the time spent by the programmer or support engineer "revising" the test program in a production environment to eliminate intermittent failures that can result from non-robust tests.

The Board Grader "Lite" procedure described here should help minimize recompile time and allow the users to more quickly focus their effort based on the data from the features of the Board Grader software. Through careful planning and organization of the testplan, the Board Grader software can provide powerful data and become one of the primary tools for the test programmer.

Appendix D: Guidelines for using Functional Test Access Ports with the Hybrid32

- The Agilent 3070 has two functional test access ports per module which are located on the ASRU card. These ports provide access for external sources and detectors to provide functional test capability beyond the built-in instruments. The functional test access ports exhibit a 50Ω (typical) characteristic impedance and a 3dB bandwidth of 12MHz (typical) to and from any Hybrid32 pincard in a module fully loaded with Hybrid32 pincards. By comparison, a fully loaded module of HybridPlus pincards will exhibit a 50Ω (typical) characteristic impedance and a 3dB bandwidth of 15MHz (typical) to and from any HybridPlus pincard.
- Test programs that utilize the ASRU Functional Test Access Ports can be identified by the presence of "connect <equipment name> signal to <functional port id>" statements in their board "config" file. The board "config" file is the "config" file located in the test program's local directory. Specific tests that utilize these ports would be powered analog tests or mixed tests with "connect" and "clear connect" statements utilizing the <equipment name> assigned to a <functional port id> in the associated board "config" file. For more details on this topic refer to the Agilent 3070 Users Manuals, Test Methods: Analog, Chapter 4: Analog Functional and Mixed Testing and the Syntax section for "connect" and "clear connect" statements as they pertain to using external test equipment.
- Tests of this type that are marginal or intermittent may not migrate to the Hybrid32 configuration without debug effort. Tests that do not appear marginal but may be close to their limits may also need some debug to migrate.
- Debug tip: Agilent 3070 Users who experience migration difficulties with existing tests using the Functional Test Access Ports when Hybrid32 cards are used should try switching from functional port AF1 to AF2 for increased performance. AF2 typically has a slightly higher 3dB bandwidth, although, the specifications always reflect the most conservative (AF1).
- Development tip: For greatest performance, new developments (in either 16 or 32 channel mode) utilizing the Functional Test Access Ports in modules containing Hybrid32 pincards should try to use the AF2 port (as compared to the AF1 port) and pincards in slots farthest away from the ASRU card (slot 11 as compared to slot 2).